REMARKS

In response to the final Office Action mailed November 15, 2004, Applicant submits the following remarks. Applicant would also like to thank Examiner Nguyen for indicating in the telephone call on January 5, 2005 that he would grant a telephonic interview to discuss the rejections of the pending claims, and the rejection of claim 1 in particular, upon receiving this response. Accordingly, Applicant requests that Examiner Nguyen call the undersigned attorney of record to schedule a telephonic interview upon receiving this response.

§ 102(b)

The Patent Office rejected claims 1, 2, 6, 10, 11, 14, 15, 17, 18, 27-29, and 32 under 35 U.S.C. § 102(b) as being anticipated by Graziadei (U.S. Patent No. 4,480,337). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 UPPQ 2d 1051, 1053 (Fed. Cir. 1987).*

Regarding claim 1, Graziadei fails to expressly or inherently disclose at least a mixer circuit comprising a gain stage coupled to receive a modulated bias current on a common node, the gain stage having a first current, a current shunt circuit coupled between the common node and a reference voltage, the current shunt circuit having a second current, wherein the first current and the second current are coupled to the common node, and a bias circuit to generate the modulated bias current.

Referring to Figure 2, Graziadei discloses a mixer and amplifier circuit including a first differential amplifier (T1-T4), a mixer differential amplifier (T5, T6), a current generator (T7), a double balanced mixer (T8-T11), and shunt transistors (T12, T13). As disclosed in col. 3, lines 46-57:

> When the average level of the input signal is high enough ..., the transistors T12 and T13 begin to conduct, effectively connecting (i.e. shunting) the input and the output of the circuit formed by the connection of the first input differential amplifier to the differential amplifier of the mixer. The shunt effect increases as the level of the signal increases, while the gain of the differential amplifiers decreases until these are completely inactive and the signal is introduced in the mixer circuit by only the transistors T12 and T13.

To ensure linear operation when the level of the RF input signal increases above a threshold, the shunt transistor (T12) shunts a common node of the transistors (T8, T9) of the double balanced mixer to the RF signal, and the shunt transistor (T13) shunts a common node of the transistors (T10, T11) of the double balanced mixer to RF signal. As a result, the RF signal, or a portion thereof, is shunted directly to the double balanced mixer, thereby bypassing the first differential amplifier (T1-T4) and reducing the gain of the system. Thus, the shunt transistors (T12, T13) operate to shunt the RF signal to common node, or input, of the double balanced mixer (T8-T11) rather than to shunt current the common node to a reference voltage. In other words, each of the shunt transistors (T12, T13) of Graziadei shunt the RF signal to the common node rather than shunt the common node to a reference voltage.

Further, in order to anticipate claim 1, Graziadei must disclose a gain stage coupled to receive a first signal, a current shunt coupled between the common node and a reference voltage, and a bias circuit having an input coupled to receive a second signal. Thus, Grazadei must disclose a first signal, a second signal, and a reference voltage. In Grazadei, the oscillator signal from the oscillator (OS) reads on the claimed first signal, the RF input signal reads on the claimed second signal, and the voltage (V_{CC}) reads on the claimed reference voltage. As such, Graziadei discloses that the shunt transistors (T12, T13) shunt the RF input signal (second signal) to the common node of transistors T8, T9 (gain stage), thereby bypassing the first differential amplifier (T1-T4). Graziadei fails to disclose a shunt circuit that shunts the common node of transistors T8, T9 to the voltage V_{CC} (reference voltage). Further, the Patent Office cannot contend that the RF input signal is the reference voltage due to element differentiation. The Patent Office cannot use the signal RF signal to show two claimed elements, namely the second signal and the reference voltage. Thus, since Graziadei fails to disclose a current shunt circuit coupled between a common node of a gain stage and a reference voltage, claim 1 is allowable.

For at least the same reason claim 1 is allowable, claims 2, 3, 5-18, and 27-32 are allowable. However, Applicant reserves the right to address the rejections of claims 2, 3, 5-18, and 27-32 in the future if necessary.

In view of the discussion above, claims 1-3, 5-18, and 27-32 are allowable. Reconsideration is respectfully requested. If any issues remain, the examiner is encouraged to contact the undersigned attorney of record to expedite allowance and issue.

Respectfully submitted,

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